The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 29

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte HAO FANG

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Appeal No. 2001-2089
Application 08/993,368

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ON BRIEF

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Before HAIRSTON, FLEMING, and RUGGIERO, Administrative Patent Judges.

RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal from the final rejection of claims 12-21, which are all of the claims pending in the present application. Claims 1-11 have been canceled.

The claimed invention relates to a NAND-type flash memory device having a core region which includes a stacked gate flash memory structure. Further included in the stacked gate flash memory structure is a conductive poly1 layer formed over a tunnel oxide layer with an insulating layer overlying the poly1 layer and a conductive poly2 layer overlying the insulating layer. The core region also includes a select gate transistor which has a gate oxide layer formed with the same insulating layer as the stacked gate flash memory structure and further includes a poly2 gate layer formed over the gate oxide layer. According to Appellant (specification, pages 3 and 4), by using, as the gate oxide layer in the select gate transistor, the same layer as the interpoly insulating layer in the stacked gate flash memory structure, a dual core oxide manufacturing process is eliminated, thereby producing a less expensive and more reliable device.

Claim 17 is illustrative of the invention and reads as follows:

17. A NAND-type flash memory device comprising:

a core region comprising a stacked gate flash memory cell structure having a thin oxide material forming a tunnel oxide layer, a first conductive material forming a poly1 layer overlying the tunnel oxide layer, an insulating material forming

an insulating layer overlying the poly1 layer and a second conductive material forming a poly2 layer overlying the insulating layer; and

the core region further comprising a select gate transistor having the same insulating layer used to form the insulating layer in the stacked gate flash memory structure to form a gate oxide layer, thus providing for the formation of the insulating layer and the gate oxide layer in a single formation step, and the second conductive material forming a gate layer overlying the gate oxide layer.

The Examiner relies on the following prior art:

Maiti et al. (Maiti)	5,861,347	Jan. 19, 1999 (filed Jul. 03, 1997)
Komori et al. (Komori)	5,904,518	May 18, 1999 (filed Jun. 30, 1997)

Masaki Momodomi et al. (Momodomi), "A 4-Mb NAND EEPROM with Tight Programmed V_t Distribution," IEEE Journal of Solid-State Circuits, Vol. 26, No. 4 (April 1991).

Claims 12-21, all of the appealed claims, stand finally rejected under 35 U.S.C. § 103(a). As evidence of obviousness, the Examiner offers Momodomi in view of Komori with respect to claims 17, 18, and 20, and adds Maiti to the basic combination with respect to claims 12-16, 19, and 21.

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the Briefs[1], the final Office action (Paper No. 18), and the Answer for the respective details.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the Examiner and the evidence of obviousness relied upon by the Examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, Appellant's arguments set forth in the Briefs along with the Examiner's rationale in support of the rejection and arguments in rebuttal set forth in the Examiner's Answer.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the invention as set forth in claims 12-21. Accordingly, we reverse.

[1] The Appeal Brief was filed October 27, 2000 (Paper No. 23). In response to the Examiner's Answer Mailed January 16, 2001 (Paper No. 24), a Reply Brief was filed March 5, 2001 (Paper No. 27), which was acknowledged and entered by the Examiner in the communication dated March 19, 2001 (Paper No. 28).

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the Examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the Examiner are an essential part

of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

With respect to independent claim 17, as the basis for the obviousness rejection, the Examiner proposes to modify the flash memory structure disclosure of Momodomi which includes a core region having a stacked gate flash memory cell and a select gate transistor. According to the Examiner (final Office action, page 3), Momodomi discloses the claimed invention except for the formation of the gate oxide of the select gate transistor with the same layer as the insulating layer of the flash memory cell, as well as a poly2 layer, as in the flash memory cell, overlying the gate oxide layer. To address this deficiency, the Examiner turns to Komori which, as asserted by the Examiner, discloses, as illustrated in Figure 1, a select transistor Qn having the same gate oxide and gate layers, identified by numerals 8 and 9, respectively, as the flash memory cell Qm. In the Examiner's analysis (id., at 4), the skilled artisan would have been motivated and found it obvious to form the gate oxide and gate layer of the flash cell and the select transistor of the device of Momodomi with the same layers ". . . to improve the electrical

reliability of the semiconductor device and to decrease the number of manufacturing steps" as suggested by Komori at column 2, lines 65-67 and column 3, lines 4-6.

Appellant's arguments in response to the obviousness rejection initially assert (Brief, pages 5-7; Reply Brief, pages 1-3) that a prima facie case of obviousness has not been established since there is no suggestion or motivation in the disclosures of the Momodomi and Komori references for the Examiner's proposed combination. In particular, Appellant contends (Brief, pages 4-7; Reply Brief, pages 1-3) that Komori, relied on by the Examiner as suggesting a select gate transistor with the requisite claimed layer structure, in fact has no teaching of select gate transistors.

After careful review of the applied Momodomi and Komori references in light of the arguments of record, we are in general agreement with Appellant's position as stated in the Briefs. While it is proper for an Examiner to consider, not only the specific teachings of a reference, but inferences a skilled artisan might draw from them, it is equally important that the teachings of prior art references be considered in their entirety. See In re Preda, 401 F.2d 825, 826, 159 USPQ 342, 344

(CCPA 1968); W.L. Gore & Associates, Inc. V. Garlock, Inc., 721 F.2d 1540, 1548, 220 USPQ 303, 311 (Fed. Cir. 1983), cert denied, 469 U.S. 851 (1984).

In particular, in order for us to accept the Examiner's conclusions in the present factual situation, we would have to improperly selectively ignore significant portions of the disclosure of the Komori reference. As pointed out by Appellant, Komori, besides having no mention whatsoever of select gate transistors, specifically designates transistor Qn, relied on by the Examiner as suggesting the claimed structure, as a peripheral circuit component (Komori, column 6, line 64 through column 7, line 3). Given the above deficiency in the disclosure of Komori, it is our opinion that any suggestion to modify the select gate transistor circuitry in a core region of the Momodomi memory structure, could not come from the peripheral transistor structure teaching in Komori, but rather only from Appellant's own disclosure.

Further, we agree with Appellant that, while features of prior art references may be combined for a different reason than that of a claimed invention, the Examiner has the burden of showing that the stated rationale for a proposed combination has

some basis in fact. In the present factual situation, no evidence is forthcoming from the Examiner that would indicate how the stated motivation rationale, i.e., increased reliability and reduction of manufacturing steps, would result from the modification of Momodomi's circuit structure with that of Komori. The Examiner must not only make requisite findings, based on the evidence of record, but must also explain the reasoning by which the findings are deemed to support the asserted conclusion. See In re Lee, 277 F.3d 1338, 1343, 61 USPQ2d 1430, 1433-34 (Fed. Cir. 2002).

In view of the above discussion, it is our view that, since all of the limitations of the appealed claims are not taught or suggested by the applied prior art Momodomi and Komori references, the Examiner has not established a prima facie case of obviousness. Accordingly, the 35 U.S.C. § 103(a) rejection of independent claim 17 and its dependent claims 18 and 20 is not sustained.

Turning to a consideration of the Examiner's 35 U.S.C. § 103(a) rejection of claims 12-16, 19, and 21 in which the Maiti reference is added to the combination of Momodomi and Komori, we do not sustain this rejection as well. Although the Examiner has

applied Maiti to address the peripheral region structure recited in these claims, we find nothing in the Maiti reference which would overcome the innate deficiencies of Momodomi and Komori discussed supra.

In conclusion, we have not sustained the Examiner's 35 U.S.C. § 103(a) rejection of any of the claims on appeal. Therefore, the decision of the Examiner rejecting claims 12-21 is reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)	
MICHAEL R. FLEMING Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
JOSEPH F. RUGGIERO Administrative Patent Judge	)	

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